layer to fill the opening therewith; and (d) forming a gate electrode on the fourth nitride semiconductor layer.

[0012] The inventive method for fabricating a nitride semiconductor device includes the step of epitaxially growing first through third nitride semiconductor layers in sequence. Thus, no interface state is formed in the interface between the second nitride semiconductor layer and the third nitride semiconductor layer. In addition, channel formed between the first nitride semiconductor layer and the second nitride semiconductor layer is kept away from the surface. Accordingly, the influence of the surface state on the channel layer is reduced, thus much more effectively suppressing occurrence of current collapse resulting from the surface state, than in a conventional method. The inventive method also includes the step of epitaxially growing a p-type fourth nitride semiconductor layer so that an opening is filled therewith. Thus, a normally-off nitride semiconductor device is easily fabricated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. **1** is a cross-sectional view illustrating a nitride semiconductor device according to a first embodiment of the present invention.

[0014] FIGS. **2**A through **2**C are cross-sectional views showing respective process steps of a method for fabricating a nitride semiconductor device according to the first embodiment in the order of fabrication.

[0015] FIGS. **3**A through **3**C are cross-sectional views showing respective process steps of the method for fabricating a nitride semiconductor device of the first embodiment in the order of fabrication.

[0016] FIG. **4** is a cross-sectional view illustrating a nitride semiconductor device according to a second embodiment of the present invention.

[0017] FIG. **5** is a cross-sectional view illustrating a nitride semiconductor device according to a first modified example of the second embodiment.

[0018] FIG. **6** is a cross-sectional view illustrating a nitride semiconductor device according to a second modified example of the second embodiment.

[0019] FIG. **7** is a cross-sectional view illustrating a nitride semiconductor device according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Embodiment 1

[0020] A first embodiment of the present invention will be described with reference to the drawings. FIG. **1** is a cross-sectional view illustrating a nitride semiconductor device according to the first embodiment. A buffer layer **12** made of AlN and having a thickness of 100 nm, a first nitride semiconductor layer **13** made of undoped GaN and having a thickness of 2 μm, a second nitride semiconductor layer **14** made of undoped AlGaN and having a thickness of 15 nm, and a third nitride semiconductor layer **15** made of n-type AlGaN and having a thickness of 30 nm are formed on a c-plane sapphire substrate **11**. The gate region of the third nitride semiconductor layer **15** has an opening in which the second nitride semiconductor layer **14** is exposed. A fourth nitride semiconductor layer **16** with a thickness of 100 nm is formed above the third nitride semiconductor layer **15** to fill the opening. A fifth nitride semiconductor layer **17** made of undoped AlGaN and having a thickness of 5 nm is formed between the fourth nitride semiconductor layer **16** and the second and third nitride semiconductor layers **14** and **15**. The term "undoped" herein means that no impurities are intentionally introduced.

[0021] A gate electrode **21** of palladium (Pd) is formed on the fourth nitride semiconductor layer **16**. The gate electrode **21** is in ohmic contact with the fourth nitride semiconductor layer **16**. Source/drain electrodes **22** and **23** are respectively formed at both sides of the gate electrode **21**. In this embodiment, the source/drain electrodes **22** and **23** are formed in recesses formed by removing the fourth nitride semiconductor layer **16**, the fifth nitride semiconductor layer **17**, and parts of the third, second and first nitride semiconductor layers **15**, **14** and **13**. In this manner, the source/drain electrodes **22** and **23** are in direct contact with two-dimensional electron gas produced near the heterojunction interface between the first nitride semiconductor layer **13** and the second nitride semiconductor layer **14**, thereby reducing the contact resistance. The source/drain electrodes **22** and **23** only need to be are a stack of a titanium (Ti) layer and an aluminum (Al) layer. The source/drain electrodes **22** and **23** are not necessarily formed in recesses, and only need to be in ohmic contact with the two-dimensional electron gas serving as channel.

[0022] Most part of the fourth nitride semiconductor layer **16** is doped with approximately 1×10^{19} cm^{-3} of magnesium (Mg). Thus, the carrier concentration is approximately 1×10^{18} cm^{-3}. However, a region immediately under the gate electrode to a depth of approximately 10 nm is doped with approximately 1×10^{20} cm^{-3} of Mg. The carrier concentration of the third nitride semiconductor layer **15** is approximately 1×10^{18} cm^{-3}.

[0023] In the nitride semiconductor device of this embodiment, the two-dimensional electron gas concentration immediately under the gate electrode is lower than that in the other region so that normally-off operation is implemented. In addition, because of the presence of the third nitride semiconductor layer **15**, channel is kept away from the surface of the semiconductor layers between the gate electrode **21** and the source electrode **22** and between the gate electrode **21** and the drain electrode **23**. Accordingly, channel is not susceptible to the influence of the surface state occurring in the surface of the semiconductor layers. As a result, occurrence of current collapse is suppressed.

[0024] The current collapse is considered to be due to electrons trapped in the surface state. In the absence of the third nitride semiconductor layer **15**, with application of a high drain bias of about several tens of voltages in the OFF state, the two-dimensional electron gas between the gate and the drain would be depleted by electrons trapped in the surface state of the second nitride semiconductor layer **14**. Since the time necessary for electron emission from the surface state is longer than that for electron capture, a depletion layer is also formed between the gate and the drain immediately after the gate is turned ON state. Accordingly, it is considered that channel does not fully open so that the channel resistance increases.

[0025] On the other hand, in the nitride semiconductor device of this embodiment including the third nitride semiconductor layer **15**, the distance between the channel and the surface state is large. Thus, even with an application of a high drain bias in the ON state, no depletion region is formed in the two-dimensional electron gas between the gate and the drain. Accordingly, the channel fully opens immediately after the gate is turned ON state, resulting in that the channel resistance does not increase.